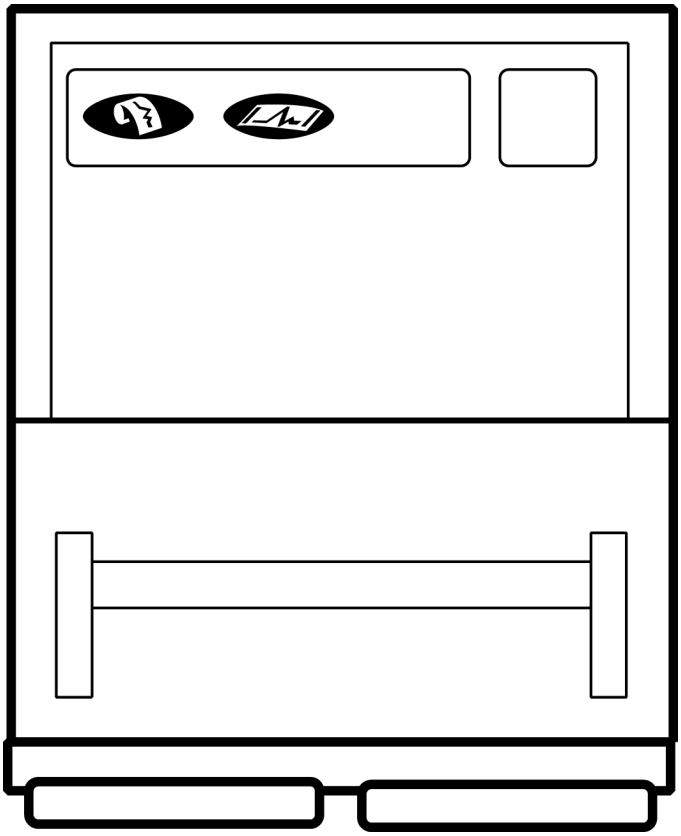
RECORDER MODULE

INTRODUCTION

This area contains service information about the Model 7335 Recorder Module. The recorder module provides numeric and waveform printouts of monitored data. Up to 2 waveforms can be traced simultaneously.



PHYSICAL DESCRIPTION

The recorder module is shown in FO-9B. The module contains a front panel with the AR-42 array recorder, rigid digital PWA, and power supply PWA. The flex cable transfers data and power from the PNet connector to the digital PWA.

FUNCTIONAL PRINCIPLES OF OPERATION

A functional block diagram of the recorder module is shown in FO-9A. The diagram is divided into digital core circuitry on the recorder digital PWA and power supply circuitry on the power supply PWA. The power supply circuitry includes the 1.0 A current limiter, storage tank, tank monitor, power supply synchronization, and the boost switching converter.

The core logic provides communication between the system host and AR-42 recorder through the PNet synchronous serial interface. It also controls all recorder functions.

Power Supply Circuits

The Recorder Module power supply provides the AR-42 recorder/printer with a source of regulated power sufficient to allow printing of images without exceeding 1.0 A mean current drain from the +12V PNet supply. Peak current may exceed 1.4 A for 50 ms or less.

Digital Circuits

Digital circuits are shown in the bottom half of FO-9A. Functional blocks include the PNet interface, reset/failsafe, 68302 CPU, 8 bit memory (RAM, flash ROM), DMA interface, and logic analyzer/test interface. Power for the core logic (+5V), is received through J100.

The Module will not be damaged when plugged into a live slot. Core logic power inputs to a module are limited to a peak inrush current during hot-plugging. Within 2 seconds the module responds to identification and wakes up in a minimized power state until registered with the system.

The PNet interface allows asynchronous and synchronous data transfer between the core logic and the external devices. Synchronous operation is always used in MPS systems. Asynchronous operation is for product development only. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafe if a problem occurs with the microprocessor. The microprocessor controls and transfers data within the core logic. The program memory is a flash ROM device that can be loaded with program information from the PNET interface or the logic analyzer interface. Data memory temporarily stores status and monitoring data for processing.

COMPONENT PRINCIPLES OF OPERATION

Recorder Module PWA schematics are contained winthin. The first sheet of schematic 315-441 shows an overall block diagram of the recorder digital PWA. Schematic 315-455 shows the recorder power supply PWA.

Recorder Power Source

The PNet interface is via connector J1. All PNet signals are passed through to the digital PWA with the exception of +12V and -12V. Interface to the digital PWA is via J2, which also provides the recorder unit printing power supply.

The MAX471 is a high side current monitor connected to the +12V PNet supply such that the current out of pin8 is proportional to the current into the source terminal of the P-Channel MOSFET (0.5mA / A). This current is converted into a voltage by a R13, giving 2.56V at an approximate 1A load. This voltage is fed via RC frequency compensation (47K, 22nF) into the positive input of one half of a TL082 Op Amp, which, along with its associated components and the 2.5V voltage reference form a closed loop control drive to the gate of the P-Channel MOSFET. The 5.1V Zener diode, 0.1uF capacitor and 10K pull-up resistor ensure that the voltage limited swing of the Op Amp output is sufficient to fully turn off the MOSFET.

Two signals from the digital PWA interface (J2) are provided for turning the MOSFET off. Both signals are diode coupled to the closed loop in such a way that when at a logic high level, the drive to the gate of the MOSFET is such that it turns off completely. The FS-1 line from the RESET-FS block of the digital PWA disables the supply under fail state. The PS_ON-0 line provides a means for the module software to control the recorder supply.

With PS_ON-0 and FS-1 at logic 0, the drain terminal of the P-Channel MOSFET behaves like a +12V, 1.0 ampere current limited power source. The loop response is set to allow rapid control of current limit even under short circuit conditions, with a maximum current overshoot up to 1.4A for less than 10mS (the main delay factor is the MAX471). Energy storage is provided by 6 3,300uF 16V electrolytic capacitors. Current from the drain of the MOSFET charges this ‘tank’ up to about 11.6V.

Diode CR12 prevents energy from the tank being returned to an unpowered acquisition unit.

The LT1170 is configured as a boost switching converter, and is supplied from the capacitor tank. It is set to maintain an output voltage of 13V, and has a single 3,300uF output capacitor to provide instantaneous current output. The output voltage can be maintained at 13V as long as the voltage on the tank remains above 3V - subject to the output load. Efficiency and current capacity drop off severely as the tank voltage drops below 5V.

The second half of the TL082 op-amp provides a status indication to the CPU via OVERI (J2-19). When the tank voltage falls below 5V OVERI goes high, and remains high until the tank voltage returns to 10.5V or above. This can be used to give an indication of power dissipation in the MOSFET, and used to shut the supply off under fault conditions.

The last block consists of circuitry to allow the LT1170 internal oscillator to be synchronized to an external clock. The LT1170 natural oscillator frequency is 100KHz. Using this synchronization circuit, its oscillator can be synchronized to between 120KHz and 160KHz.

Core Logic

The core logic is shown on the 315-441 schematic. The core logic provides communication between the system host and module through the PNet synchronous serial interface. The module is an 8-bit version of the core logic with one 128Kx8 RAM and 128Kx8 flash ROM. The microprocessor runs at 8.064 MHz.

PNet Interface

The PNet interface, shown on sheets 2 and 3 of the schematic, provides the following functions:

- RS485 drivers (U7 and U8) for serial data and clock,
- Module select and presence detection (U2),
- Module reset (U6 and U9), and
- Module synchronization.

Core signals are received on PNet connector J100 (sheet 1) with the following pin-out:

PIN	NAME	PIN	NAME
1A,1B	+5V	6B	M_SELECT
2A	DATA+	7A	M_PRESENT
2B	DATA-	7B	TXOC-0
3A,3B	+3.3V	8A	M_SYNC-0
4A	CLK+	8B	-12V
4B	CLK-	10A,10B	+12V
5A,5B	GROUND	1,2	GROUND
6A	M_RESET		

The Recorder module is designed to be inserted and removed ('hot-plugged') from powered systems. Ground pins 1 and 2 are longer than the other connector pins, thus they make first and break last to protect circuitry. This is partially because of protective impedance located on the system backplane, in series with the modules +5V and +12V power. Also series impedance on PNet control lines limits inrush and protects logic devices from excessive currents during a hot-plug power up.

The PNet protocol defines two modes of operation: synchronous and asynchronous. The normal mode of operation is synchronous, with half duplex transmitted and received data on differential signals DATA+ and DATA-. The device transmitting the serial data also generates differential clock signals CLK+ and CLK-. Transceiver direction for data and clock are controlled by the 68302 processor-generated TX_EN-0 (low true transmit enable) signal through U2. In the synchronous mode, both data and clock transceivers U7 and U8 are set to receive (i.e., transmit disabled) when fail-safe signal FS-0 is asserted.

The alternate serial mode, full duplex asynchronous, is entered by asserting processor generated control bit ASYCH_EN. This mode transmits data onto the differential signals CLK+ and CLK-, and receives data from the differential signals DATA+ and DATA-. The transmitter in the module is disabled unless the module has been commanded to transmit per the PNet protocol. The module transmitter is immediately disabled after the last character of a transmission has been sent.

The module select input (M_SELECT, hi true) instructs the module to respond to identification requests. When both M_SELECT input and M_RESET input (hi true) are asserted, the module performs a hardware reset.

The module present output, M_PRESENT is connected to M_SELECT through diode CR1 to allow a means of determining if the module is plugged in. When M_SELECT is asserted (pulled hi) M_PRESENT is hi true.

A low true open collector signal TXOC-0 from Q1 signifies the module transmitter is enabled. Serial data is then transmitted in the synchronous mode.

Reset Logic

The reset logic is shown on sheet 3 of the schematic. Power on reset is generated by U9 when the unit is powered up. Processor reset (RESET-0) and halt (HALT-0) are generated by the system. RESET-0 AND HALT-0 signals remain low for minimum of 130 msec after the logic rail is in specification.

External reset, processor reset, and halt signals are low for minimum of 24 clocks when external reset asserted. Power monitoring causes processor reset, and causes halt signals to go low when the logic rail drops below specification.

The reset circuit (U6-4,5,6; U6-11,12,13) provides open drain outputs to the processor bi-directional reset and halt signals.

Fail-Safe Logic

Fail-safe latch (U6-1,2,3; U6-8,9,10 on sheet 3) ensures that the module enters a safe state should the processor fail to operate correctly. The latch is set by a low true output from the processor watchdog timer (WDOG-0). The data transmitter is disabled and module remains in a safe state until the latch is cleared by a power on or external reset.

Microprocessor

The core logic design is based around the 68302 microprocessor (U10) shown on sheet 4 of the schematic. The 68302 combines a 68000 core with a three channel communication processor, and system integration circuits.

The left side of the CPU contains clock interfaces to/from the PNet, port A, and port B to various circuits in the core logic, reset, and halt interface. The IRQ ports are not used. The right side of the CPU contains address and data lines and chip select outputs. The 68302 operates with a statically defined 8-bit wide bus. The following resources are used for specific module functions:

CHIP SELECTS LOGIC

CS0-0	FLASH ROM
CS1-0	STATIC RAM
CS2-0	RECORDER READ
CS3-0	RECORDER WRITE

SERIAL COMM CHANNELS

SCC1	PNET [RXD1, TXD1, RCLK1, TCLK1, CTS1-0, RTS1-0]
SCC2	ASYNC DEBUG [RXD2,TXD2]
SCP	SERIAL EEPROM [SPRXD,SPTXD,SPCLK]
TIMER1	SYSTEM TIMEBASE

PARALLEL IO / SPECIAL PURPOSE IO BITS

PA2	CHIP SELECT TO SERIAL EEPROM
PA5	ASYCN_EN (PNET MODE SELECT)
PA6	POWER MANAGEMENT CONTROL
PB5 /TIN2	TIMEBASE INPUT FOR EXTERNAL MEMORY / SYSTEM CONFIG
PB7	WATCHDOG TIMER OUTPUT

Program Memory

Program memory consists of 8-bit flash ROM U11 shown on sheet 5 of the schematic. The ROM is configured for 128Kx8 (1024k bit). The ROM is not socketed and can not be removed for programming. The ROM can be flash-programmed via the logic analyzer interface or the PNET connector.

Data Memory

Data is stored in 128Kx8 static RAM U3. The RAM contents are lost when power is removed.

Non-Volatile Memory

Serial EEPROM U1 is a 128-byte PROM that provides non-volatile storage for model information and parameter user interface data which must travel with the module. The 68302 synchronous communication port (SCP) is used to access the EEPROM.

Logic Analyzer/Test Interface

The logic analyzer/test interface is shown on sheet 6 of the schematic. The core logic includes an interface to bring signals required for external ROM access, logic analyzer interface, and a debug serial channel to a single connector.

The external ROM access allows an off board ROM (8 bit) or ROMs (16 bit) to replace the flash ROM devices at address 0. Address, data, and control signals required for this function are included on the LA/T connector.

All signals needed for a Hewlett Packard model 16500 logic analyzer or equivalent to perform bus state analysis and disassembly are included on the LA/T connector.

The 68302 SCC2 serial transmit and receive data signals are included on the LA/T connector.

DMA Interface

Part of U100 implements an asynchronous state machine that interfaces the recorder unit SYNC-0 and WRRDY-0 signals to the 68302 signals DREQ-0, DONE-0, CS3-0, and output port PA12 (MODE bit). The IDMA is configured for level sensitive burst transfer, and the MODE bit (PA12) set for edge (LOW) or level (HIGH) sens on SYNC-0.

DREQ-0 is asserted on the falling edge of the WRRDY-0 signal and cleared by the falling edge of CS3-0. The only exception to this cycle is that in EDGE mode, if WRRDY-0 is already low when SYNC-0 falls, then a DREQ-0 cycle is initiated without looking for an edge on WRRDY-0.

In EDGE mode (MODE = 0), a DMA burst transfer (DREQ-0 Cycles) is synchronized to begin at the next falling edge of the SYNC-0 signal and continue up to the assertion of DONE-0 at the end of data transfer, when the state machine starts searching for the next falling edge of SYNC-0.

In LEVEL mode (MODE = 1), consecutive DMA bursts will be started whenever the SYNC-0 signal is low. Once started, a DMA transfer executes fully, as long as the recorder issues WRRDY signals, even if SYNC-0 rises prior to its completion.

The LA/T connector pinouts are as follows:

PIN	NAME	PIN	NAME
1,69	+5V	2,28,45, 46,70	GND
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
29	D0	30	D1
31	D2	32	D3
33	D4	34	D5
35	D6	36	D7
37	D8	38	D9
39	D10	40	D11
41	D12	42	D13
43	D14	44	D15
47	DTACK-0	48	AS-0
49	RW	50	UDS-0
51	DS-0	52	BGACK-0
53	FC0	54	FC1
55	FC2	56	DEBUG TXD
57	DEBUGRXD	58	EXROMCS-0
63	PRGM_EN	64	DISCPU
65	T1_IN		

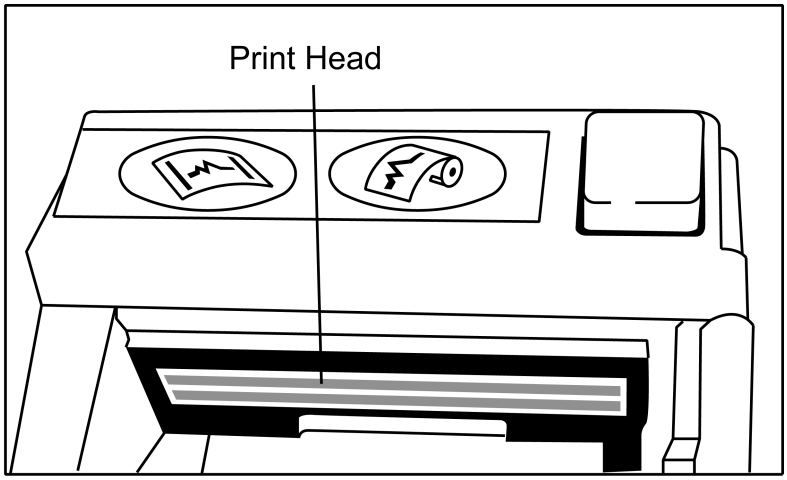
PAPER LOADING

Proceed as follows to load paper (Reorder No. 8730) in the recorder drive:

1. Open the recorder drive front door by pressing the door latch. Pull the door completely open.

2. Remove the empty paper core.

3. Place a new paper roll between the tabs of the paper holder. Ensure that the sensitive (shiny) side of the paper is facing the printhead at the top of the recorder drive (shown below) when the paper is pulled toward the door.



Recorder Module Printhead Location

4. Align the paper with the pinch roller of the door.

5. Begin to close the door while still holding onto and pulling out about 3 inches (8 cm) of paper, then close the door completely. The door latch is engaged with a snap.

6. Ensure the paper is properly aligned in the slot.

TROUBLESHOOTING

Some common recorder problems and their likely remedies are listed in Table 9-1. If problems persist, replacement of the recorder drive or digital PWA may be required.

Table 9-1. Recorder Module Troubleshooting

Problem	Remedy
Recorder moves paper, but does not print	Review paper loading procedure (paragraph 9.5) to see if paper is loaded backwards
Printouts have sections missing	Make sure printhead is clean. If there are any dropout areas, clean the print head (Figure 9-1) using a cotton swab soaked with isopropyl alcohol.
Printout appears light or uneven	Make sure wrong paper is not being used. Use paper Reorder No. 8730
Printing error messages appear	Refer to Monitor Service Manual for interpretation of printing error codes

DISASSEMBLY PROCEDURE

STATIC DISCHARGE CAUTION

Do not attempt to service unit without static discharge protection. Workstations and personnel must be properly grounded, or damage to equipment will result.

1. Remove three 6-32 screws from the rear of the Module.
2. Carefully remove rear cover assembly while disconnecting ribbon cable from power supply PWA.
3. Remove two 4-40 screws, and separate power supply PWA from rear cover.
4. Slide the enclosure away from the front panel.
5. Remove three 6-32 standoffs.
6. Unplug and remove digital PWA from recorder assembly.
7. Using FO-9B as a guide, perform any additional disassembly that may be required for maintenance procedures.

REASSEMBLY PROCEDURE

1. Join digital PWA (3, FO-9B) to recorder assembly while mating interface connector and receptacle.

2. Apply threadlock to three 6-32 x 1.16” standoffs (9), and secure digital PWA. Torque three standoffs to 6-in/lb.

3. With enclosure oriented so large grooves are at bottom and label is at right (viewed from front of Module), slide enclosure over recorder assembly.

4. Attach power supply PWA (4) to rear cover with two 4-40 x 1/4” screws (7). Torque the two screws to 4-in/lb.

5. Connect digital PWA ribbon cable to connector of power supply PWA.

6. Apply threadlock to three 6-32 x 1/2” screws (8), and attach rear cover assembly. Torque the three screws to 6-in/lb.

PARTS LISTS

Top Assembly 7335 parts are listed in Table 9-2 and shown in FO-9B. Recorder Digital PWA 315-441 parts are listed in Table 9-3 and shown in FO-9C. Recorder Power Supply PWA 315-455 parts are listed in Table 9-4 and shown in FO-9D.

Table 9-2. Top Assembly 7335 Parts List

Item	Description	Part No.
1	COVER, PARAMETER, REAR, RECORDER	703-191
2	SUB-ASSY, ENCLOSURE, EXTRUDED, RECORDER	320-677
3	PWA, RECORDER DIGITAL	315-441
4	PWA, RECORDER POWER SUPPLY	315-455
5	RECORDER ASSY, THERMAL ARRAY	320-668
7	SCREW, 4-40X1/4 PNH PHH SST	719-102
8	SCREW, 6-32X1/2 PNH PHH SST	719-439
9	STANDOFF, 6-32 X 1.16 M/F SST	735-324

Table 9-3. Recorder Digital PWA 315-441 Parts List

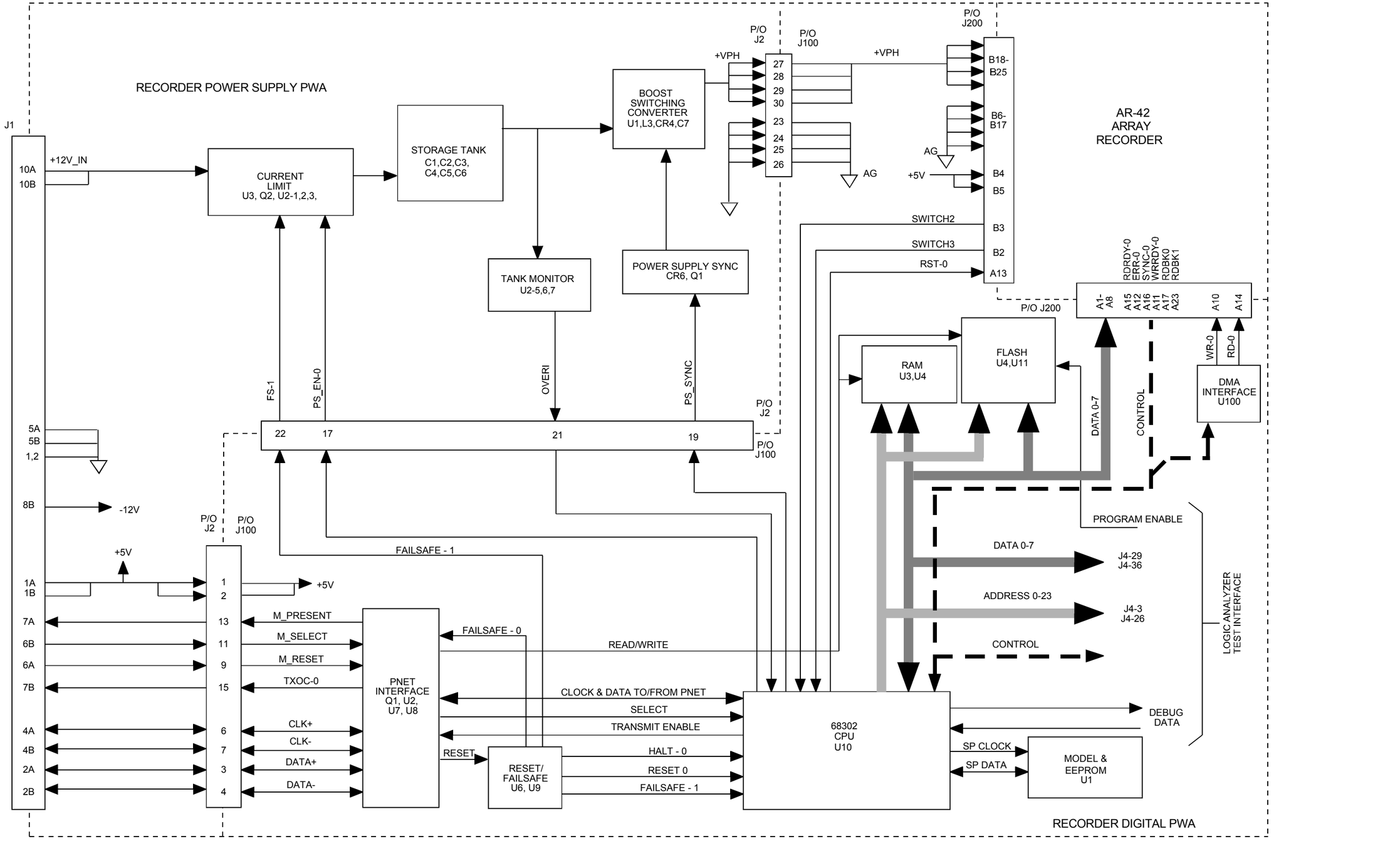
Item	Description	Part No.
C2, 3	CAP,CER,SMD,0805,NPO,10%,50V,27 PF	605-418
C4-14, 16, 100	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
CR1, 13	DIODE, SCHOTTKY, 30V, 200MW, SOT-23	611-137
CR2-7, 10, 11	DIODE, DUAL SERIES SMT SOT-23	611-140
CR12	DIO ZENER 6.2V, 5% SMT, 225MW	612-147
FB1-9, 100, 115-134	FERRITE CHIP, EMI SUPPRESSION, SMT	669-170
J4	SOCKET, MICRO STRIP 35X2, SMD	607-816
J100	CONN, CABLE FLEX, FLAT, 30 PIN	608-302
J200	CONN, 2X25, SOCKET, PC MT, STRAIGHT	607-848
Q1	XST NPN 2222A SMT	674-127
R1, 40, 41, 44, 50, 101, 102	RES,SMD,1/10W,1%,1.00K OHM	685-293
R2	RES,SMD,1/10W,1%,4.99K OHM	685-360
R3, 4, 7-33, 35, 42, 43, 46-48	RES,SMD,1/10W,1%,10.0K OHM	685-389
R5, 6	RES,SMD,1/10W,1%,2.21K OHM	685-326
R34	RES,SMD,1/10W,1%,698K OHM	685-566
R45	RES,SMD,1/10W,1%,100 OHM	685-197
R100, 103, 105-113	RES,SMD,1/10W,1%,47.5K OHM	685-454
R104	RES,SMD,1/10W,1%,499 OHM	685-264
U1	IC,93C56 2KBIT SERIAL EEPROM,CMOS SM	692-183
U2, 100	IC, EECMOS PLD 16V8B, ARRAY LOGIC	692-226
U3	IC, 128X8 70NS CMOS SRAM TSOP	694-133
U4	IC,74AC32 QUAD 2 IN OR GATE,ADV CMOS SM	692-141
U6	IC,74HC03 QUAD 2 IN.NAND,CMOS SUF MT	692-139
U7, 8	IC, CMOS LTC1485, DIFF BUS XCEIVER SO8	692-225
U9	IC, POWER SUPPLY MONT WITH RESET SMT	694-118
U10	IC, 68302 INTEGRATED PROCESSOR 144 SMT	694-130
U11	IC, 128K X 8-BIT 5V FLASH ROM CMOS SMT	692-195
Y100	CRYSTAL, 8.064MHZ, HC-49/UP	609-134
#28	PAL_U2A, CORE LOGIC	637-101
#30	PAL_U100, RECORDER INTERFACE	637-103

Table 9-4. Recorder Power Supply PWA 315-455 Parts List

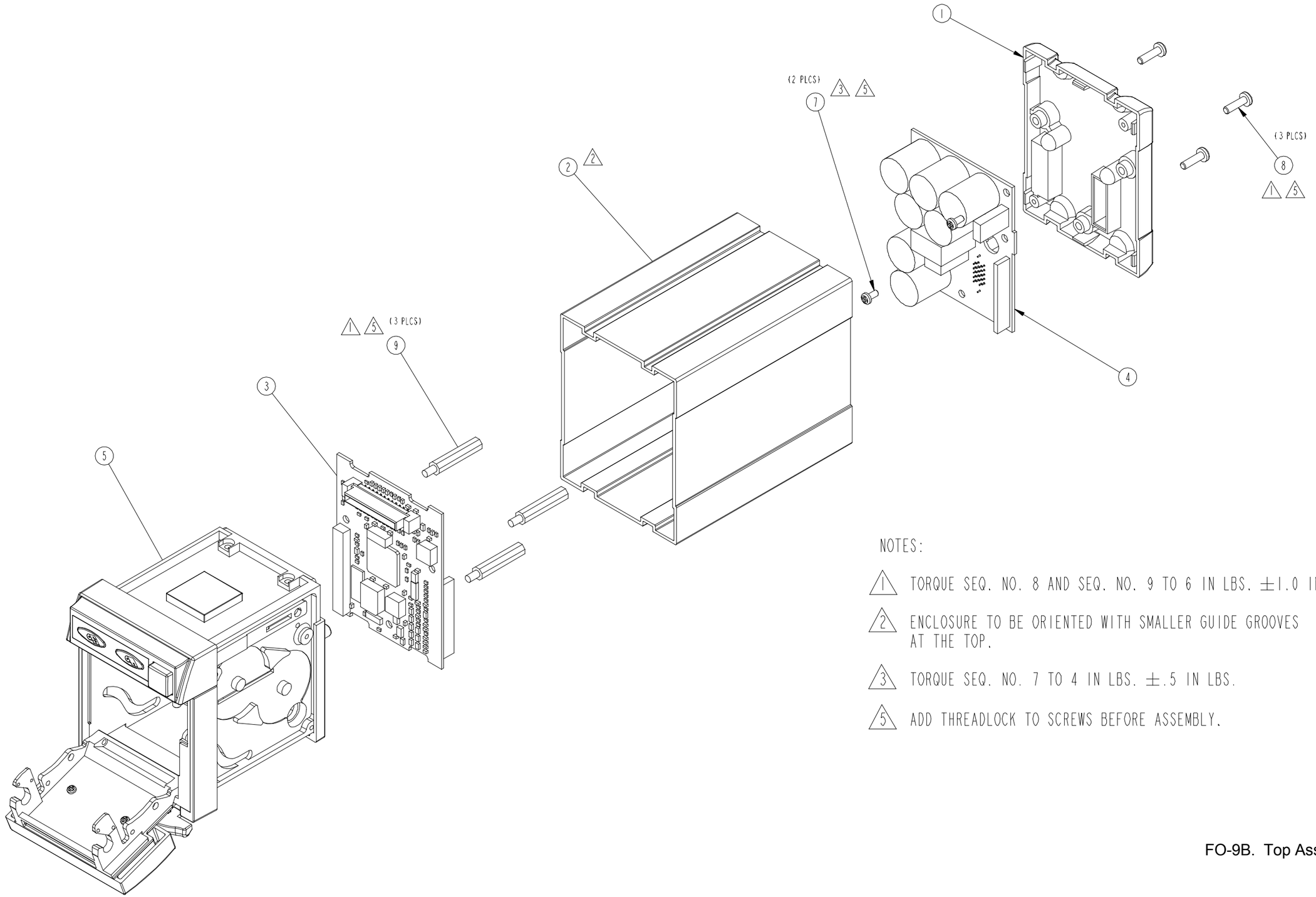
Item	Description	Part No.
C1-7	CAP, ELECTROLYTIC 3300UF, 16V, 20%	603-216 or 604-192
C8	CAP,CERAMIC,SMD,Z5U,50V,0.022 UF	605-317
C9	CAP,CER,SMD,0805,X7R,10%,50V,0.033 UF	605-527
C10-13, 19	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C15	CAP,0805,CER,NPO,5%,50V,100PF	603-624
C16	CAP,2917/D,TANT,20V,20%,22UF	606-136
C18	CAP,2312/C,TANT,16V,20%,10 UF	606-108
C20	CAP,2917/D,TANT,35V,20%,10 UF	606-188
C21	CAP,2917/D,TANT,35V,20%,4.7UF	606-186
CR1, CR11	DIO, ZENER,5.1V,5%,225MW SURFACE MOUNT	612-145
CR2	DIO ZENER 4.3V,5%,350MW SURFACE MOUNT	612-131
CR3	DIODE, DUAL SERIES SMT SOT-23	611-140
CR4	DIODE, MBRD340, SCHOTTKY BARRIER, SMT	610-115
CR5, 6, 8, 9	DIO SWI, 200 MA, 70V, SMD	610-114
CR10	IC, VOLTAGE REF, 2.5V PRECISION, SO8	621-251
CR12	DIODE, RECT-SCHOTTKY, 1A, 40V, SMT	611-142
J1	CONN, 20 PIN PLUG STRAIGHT PC MOUNT	607-794
J2	CONN, 30 PIN, 050 PITCH, SIP HDR	607-839
L3	INDUCTOR, TOROIDAL, 50UH, 10%, 2A	669-190
Q1	XSTR, N-CHAN MOS SOT-23	676-130
Q2	XSTR, TMOS P FET POWER MTD 2955E SMT	674-141
R1	RES,SMD,1/10W,1%,221 OHM	685-230
R2	RES,SMD,1/10W,1%,499K OHM	685-552
R4, 11	RES,SMD,1/10W,1%,47.5K OHM	685-454
R6	RES,SMD,1/10W,1%,11.8K OHM	685-396
R7	RES,SMD,1/10W,1%,3.65K OHM	685-347
R10	RES,SMD,1/10W,1%,237K OHM	685-521
R12, 22	RES,SMD,1/10W,1%,100K OHM	685-485
R13	RES,SMD,1/10W,1%,4.99K OHM	685-360
R15	RES,SMD,1/10W,1%,4.75K OHM	685-358
R16	RES,SMD,1/10W,1%,1.24K OHM	685-302
R17	RES,SMD,1/10W,1%,1.00K OHM	685-293
R18, 24	RES,SMD,1/10W,1%,100 OHM	685-197
R19	RES,SMD,1/10W,1%,2.21K OHM	685-326
R20, 21	RES,SMD,1/10W,1%,10.0K OHM	685-389
R23	RES,SMD,1/10W,1%,210K OHM	685-516

Table 9-4. Recorder Power Supply PWA 315-455 Parts List (Continued)

Item	Description	Part No.
TP1	CONN, 1 POSN HEADER, .025 SQ	608-288
U1	IC, SWITCHING REGULATOR, 5A	621-257
U2	IC, DUAL JFET OP AMP SOIC	691-110
U3	IC, HIGH SIDE CURRENT SENSE AMP SMT	691-132
#46	TYWRAP NYLON .75 BDL DIA.MAX.	756-101



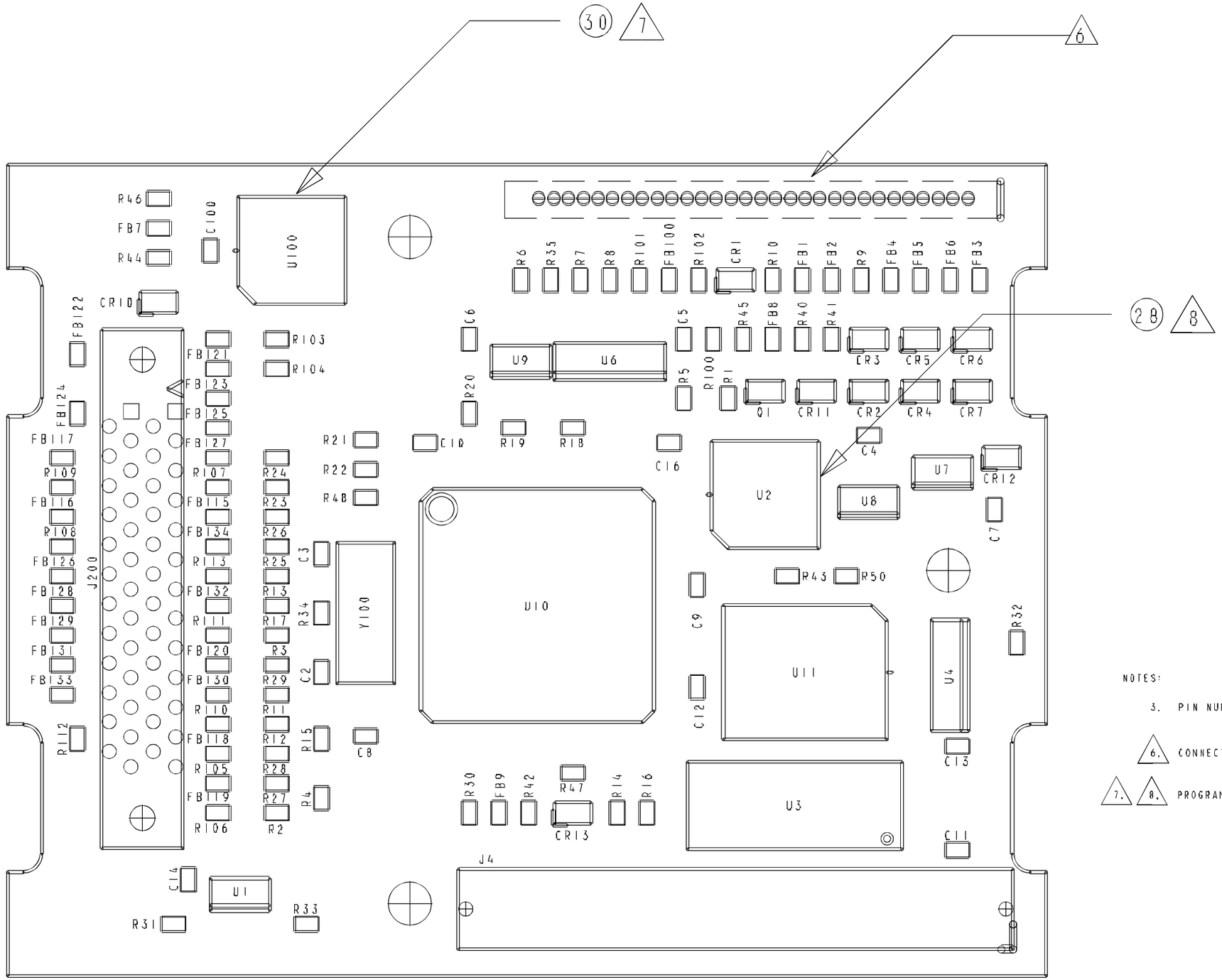
FO-9A. Recorder Module Block Diagram



NOTES:

1. TORQUE SEQ. NO. 8 AND SEQ. NO. 9 TO 6 IN LBS. ±1.0 IN LBS.
2. ENCLOSURE TO BE ORIENTED WITH SMALLER GUIDE GROOVES AT THE TOP.
3. TORQUE SEQ. NO. 7 TO 4 IN LBS. ±.5 IN LBS.
5. ADD THREADLOCK TO SCREWS BEFORE ASSEMBLY.

FO-9B. Top Assembly 7335



NOTES:

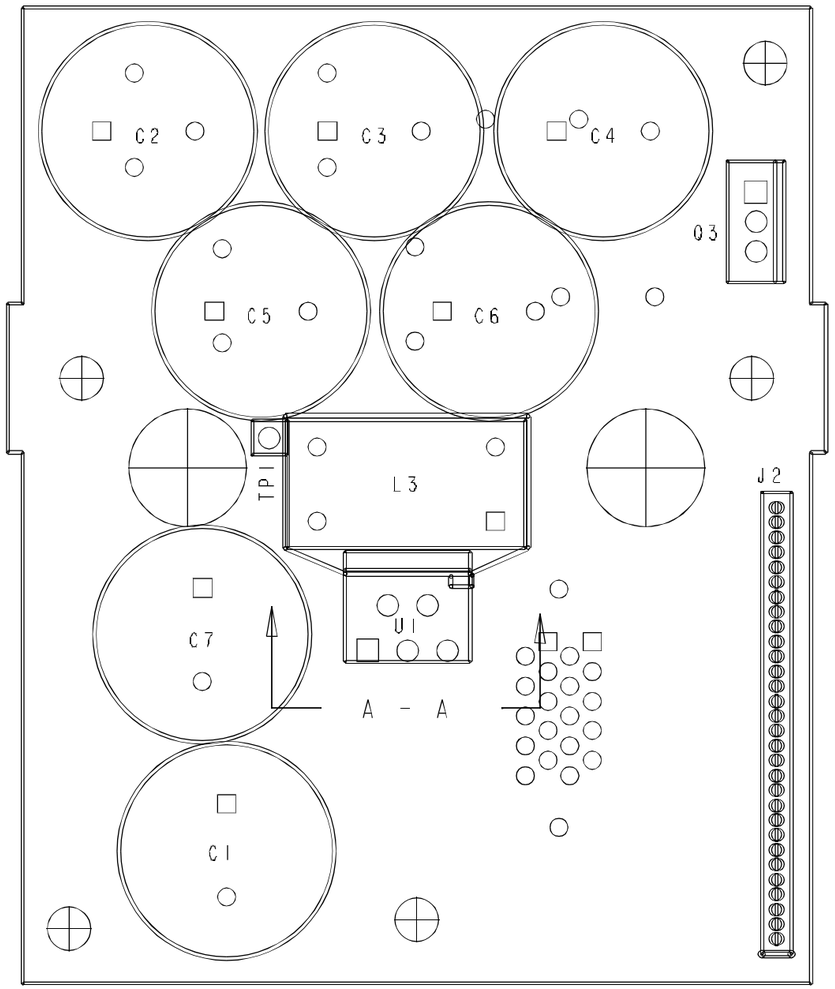
3. PIN NUMBER 1 IS INDICATED BY MARKINGS.

6. CONNECTOR J100 TO BE MOUNTED ON SECONDARY SIDE OF BOARD.

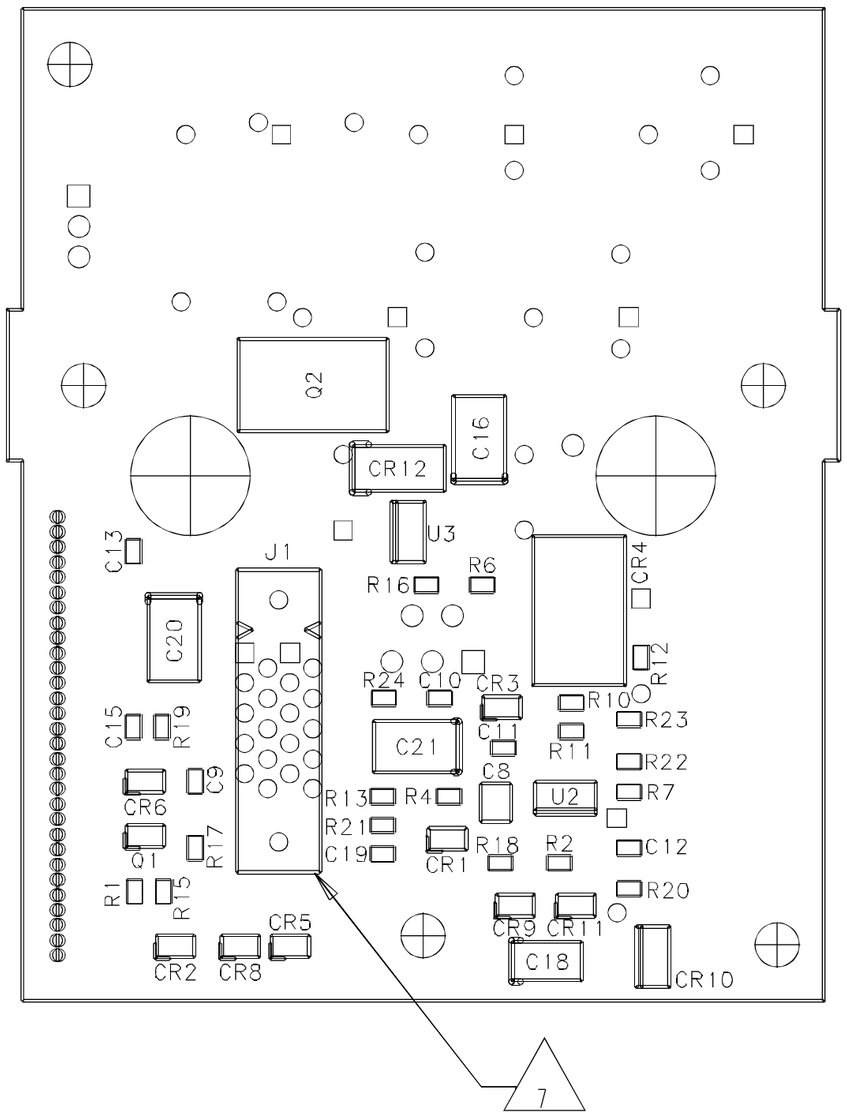
7. 8. PROGRAM DEVICE PRIOR TO INSTALLATION.

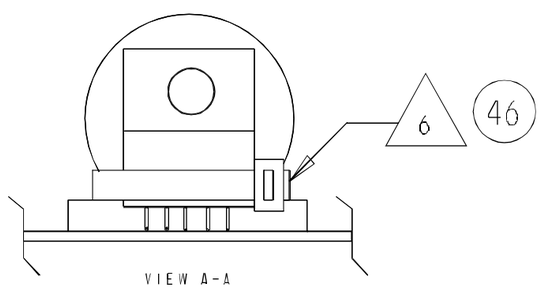
FO-9C. Recorder Digital PWA 315-441

PRIMARY SIDE



SECONDARY SIDE





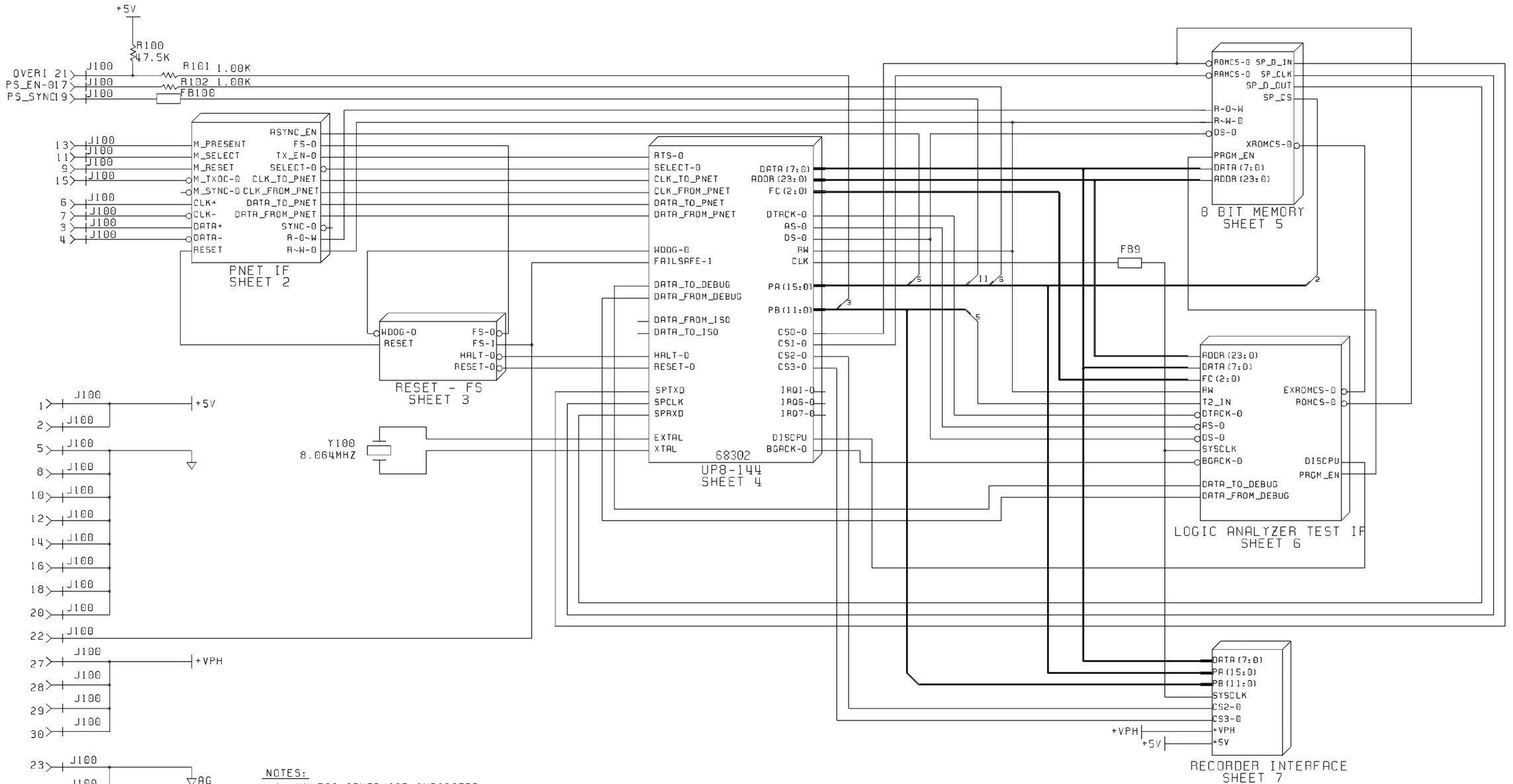
NOTES:

3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

△6 SECURE DEVICE TO INDUCTOR WITH TYWRAP(SEQ NO. 46).
TIGHTEN TYWRAP WITH McMASTER CARR P/N7139K75 CABLE TIE TOOL OR EQUIVALENT.

△7 ENSURE J1 IS MOUNTED FLUSH TO THE BOARD.

FO-9D. Recorder Power Supply PWA 315-455

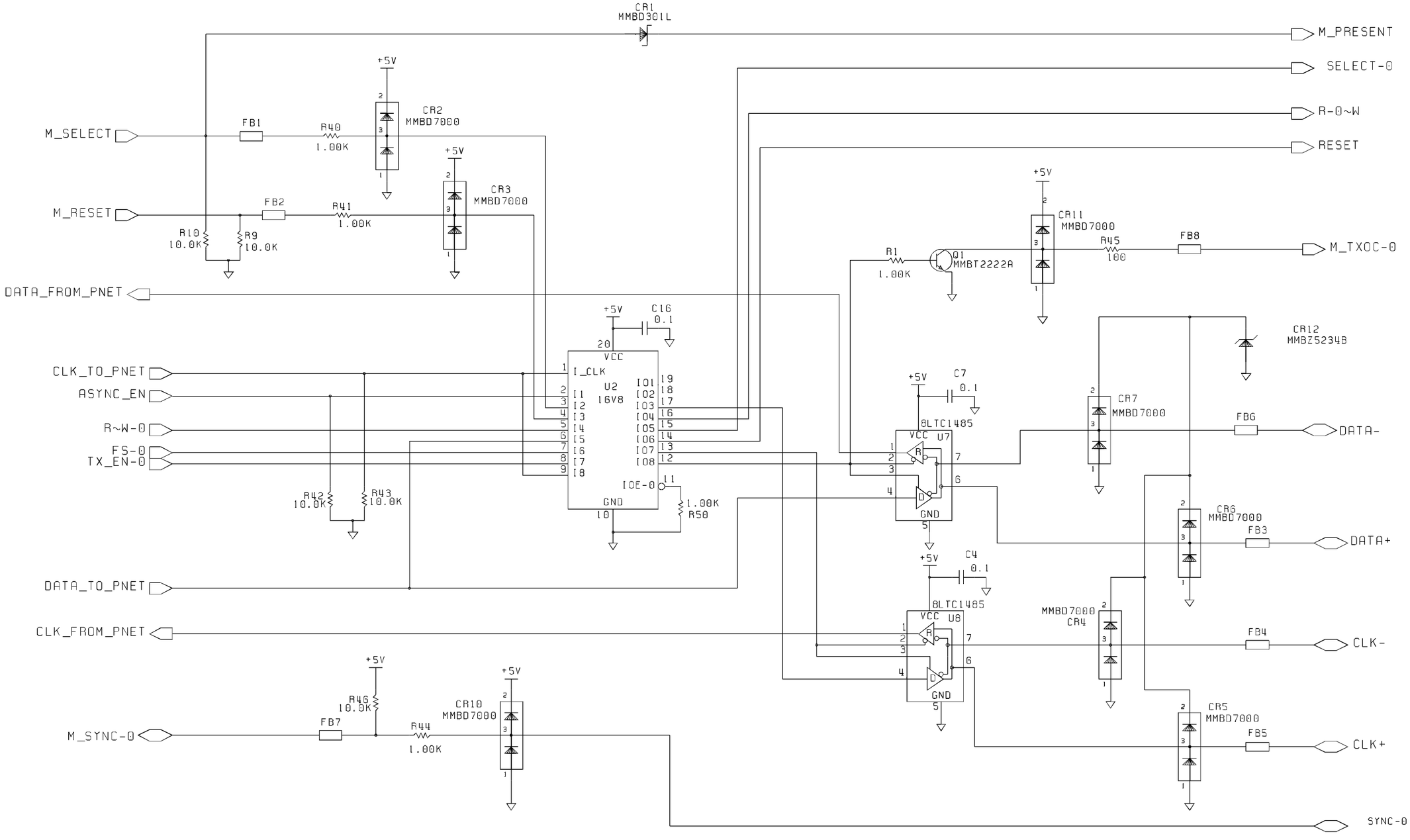


NOTES:

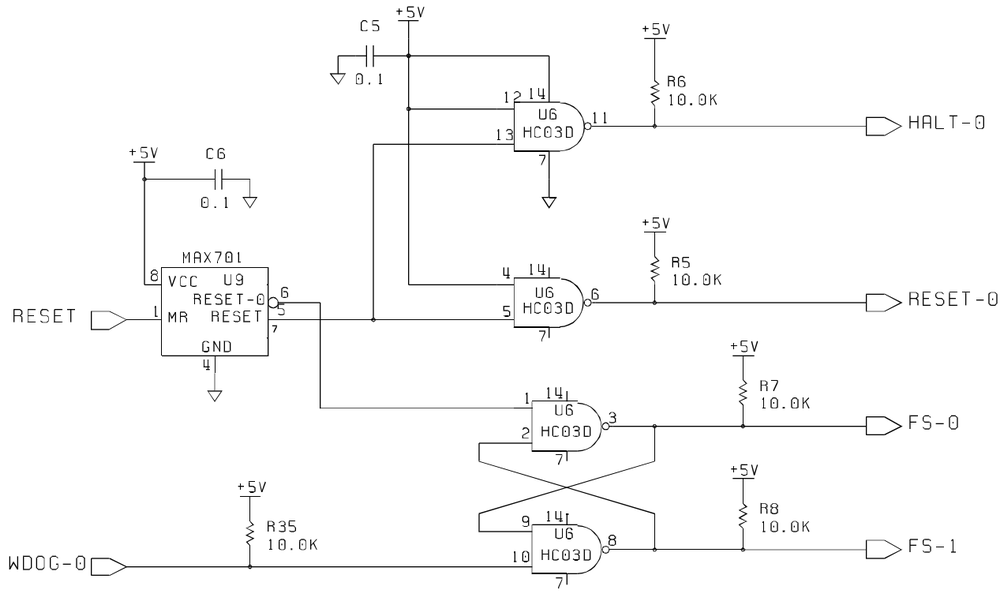
1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS. +/-1%.1/10W
   B. CAPACITORS ARE IN MICROFARADS. +/-10%
   C. INDUCTORS ARE IN MICROHENRYS. +/-10%

2. REFERNCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C2 TO C14,C16,C100,CR1 TO CR7,CR10 TO CR13,FB1 TO FB9,FB100,FB115 TO FB134,J4,J100,J200,Q1,R1 TO R35,R40 TO R48, R50,R100 TO R113,U1 TO U4,U6 TO U11,U100,Y100
   B. REFERENCE DESIGNATORS NOT USED:
      C1,C15,C17 TO C99,CR8,CR9,FB10 TO FB99,FB101 TO FB114,J1 TO J3,J5 TO J99,J101 TO J199,R36 TO R39,R49,R51 TO R99,U5,U12 TO U99,Y1 TO Y99.

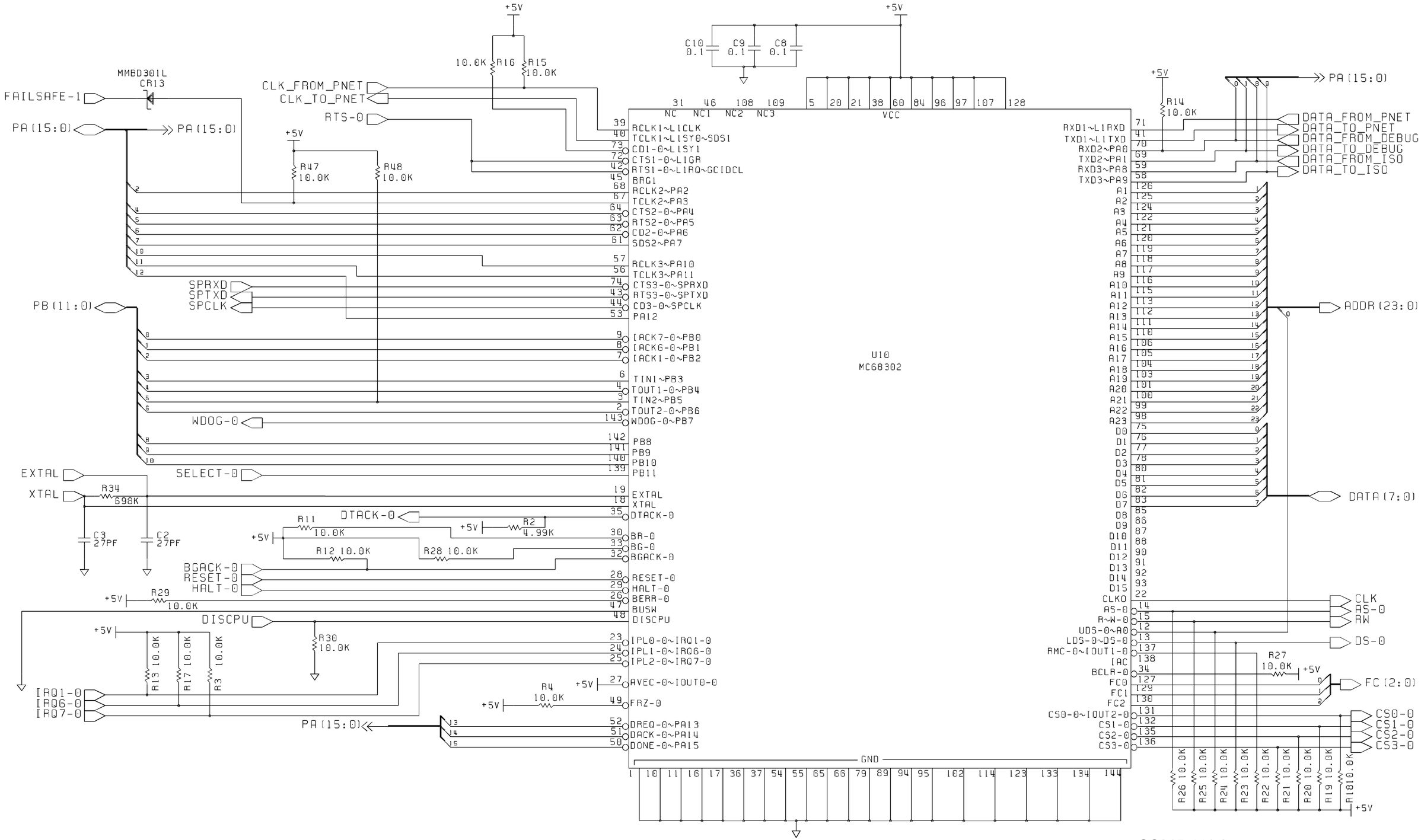
SC315-441 A
Recorder Digital PWA Schematic (1 of 7)



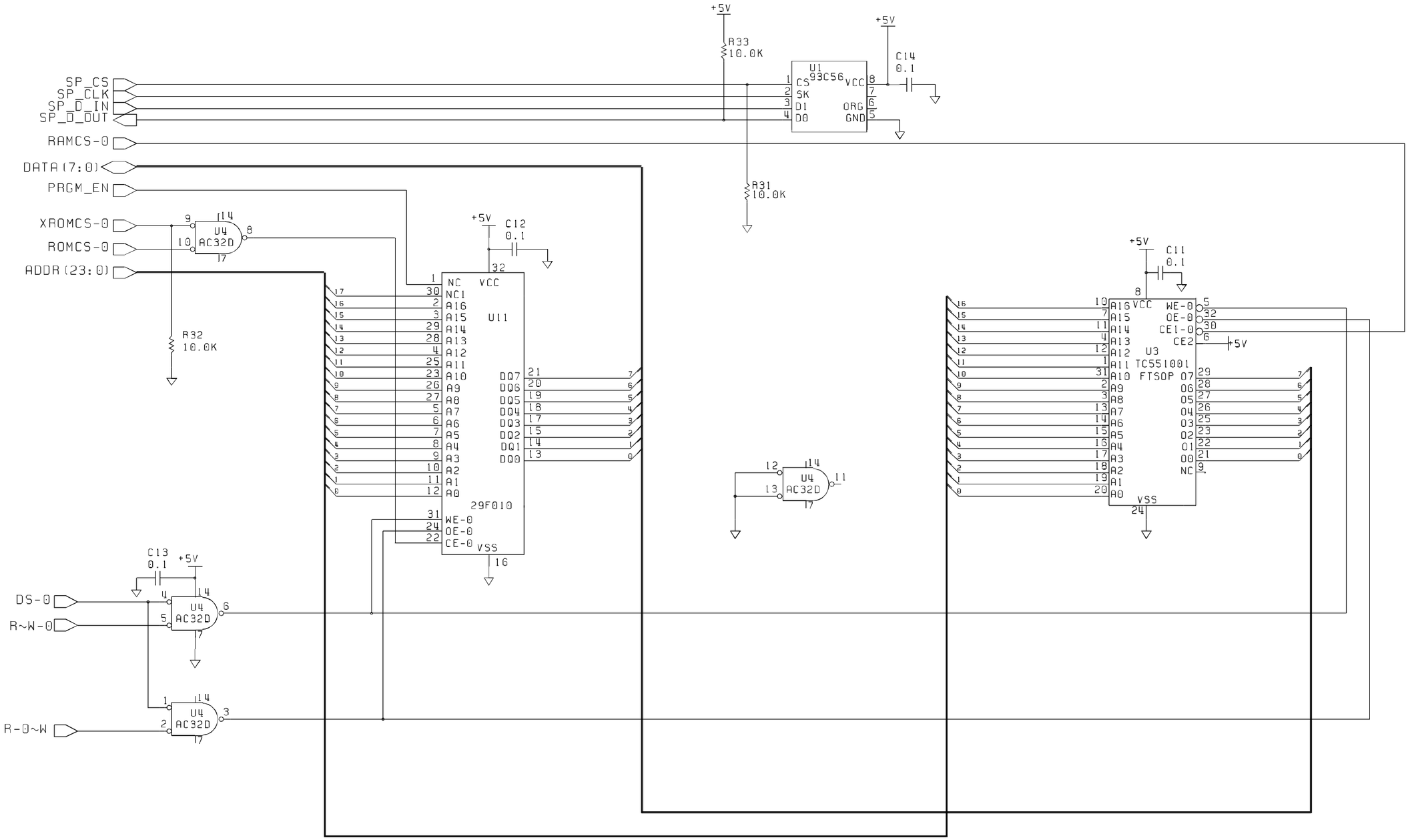
SC315-441 A
Recorder Digital PWA Schematic (2 of 7)



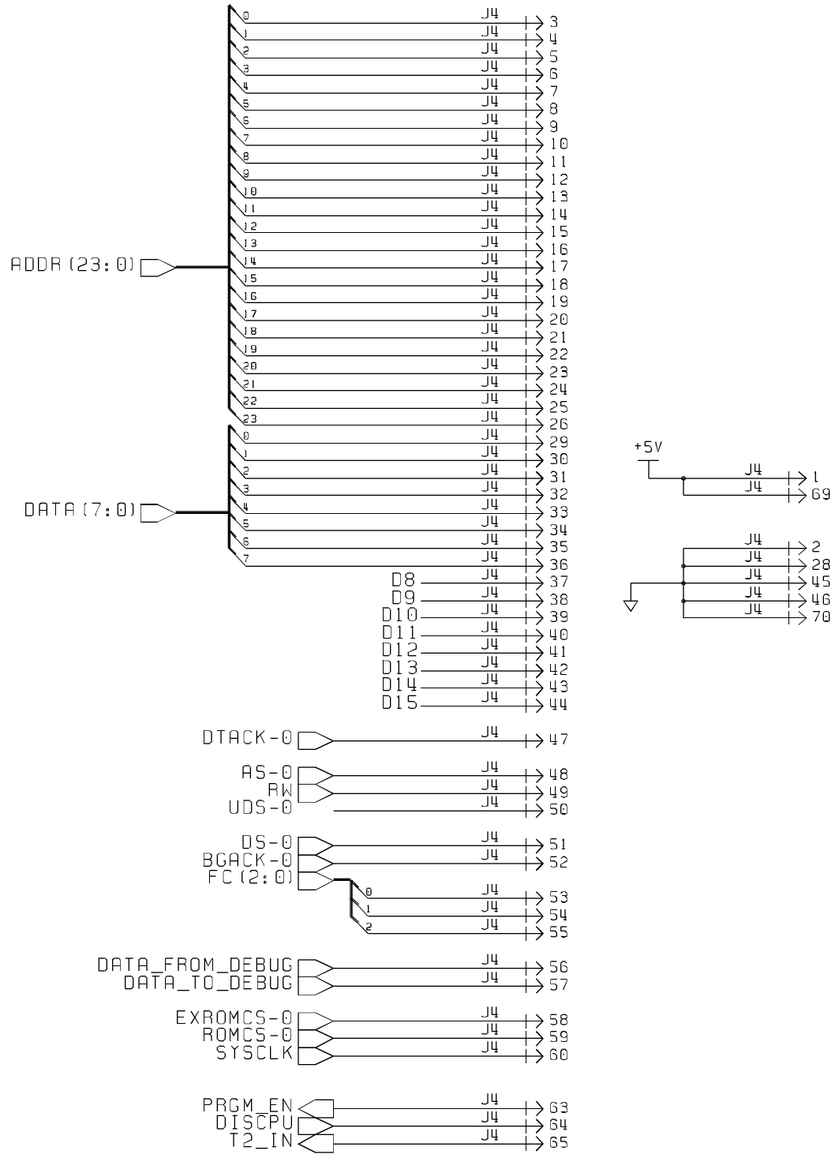
SC315-441 A
Recorder Digital PWA Schematic (3 of 7)



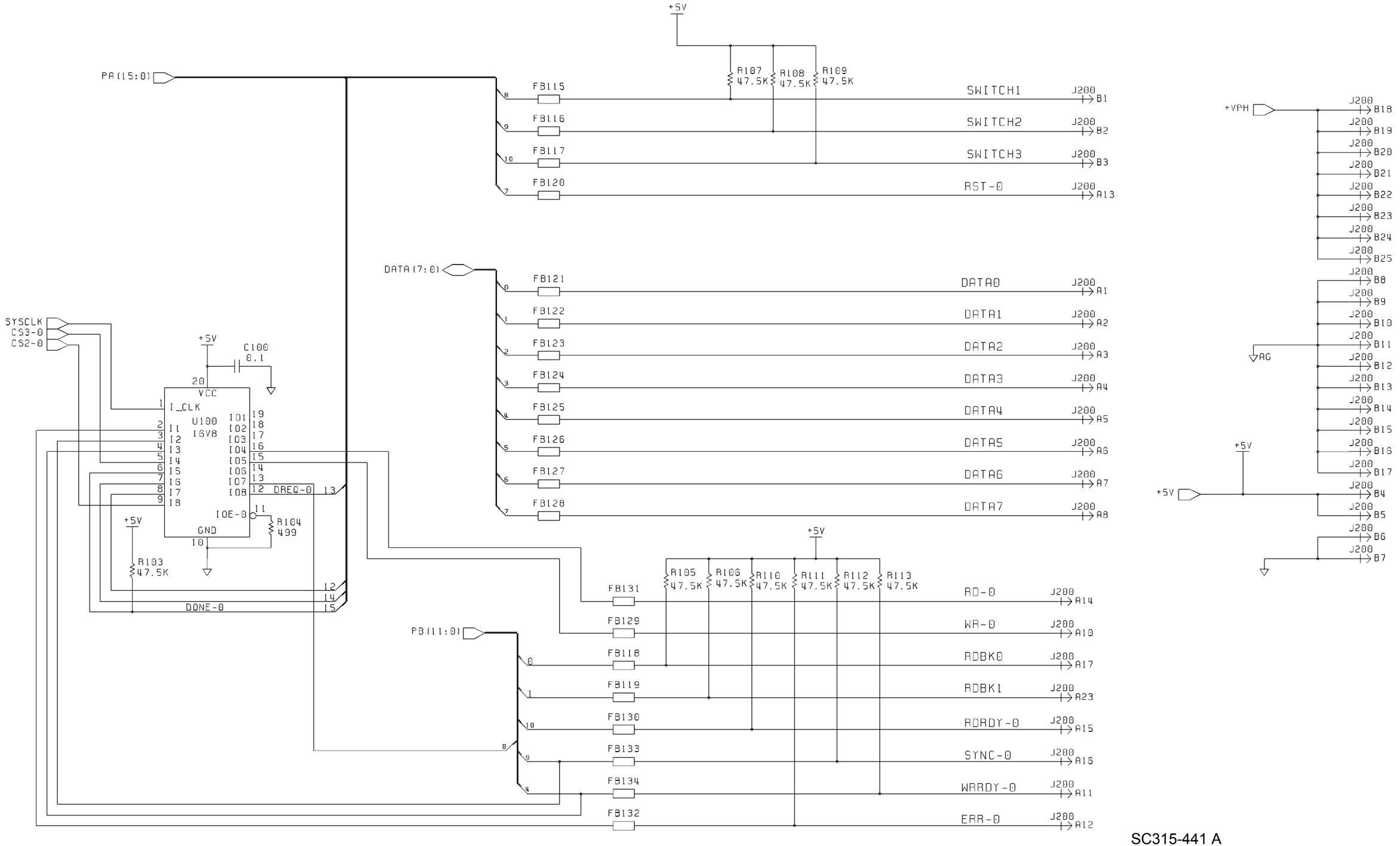
SC315-441 A
Recorder Digital PWA Schematic (4 of 7)



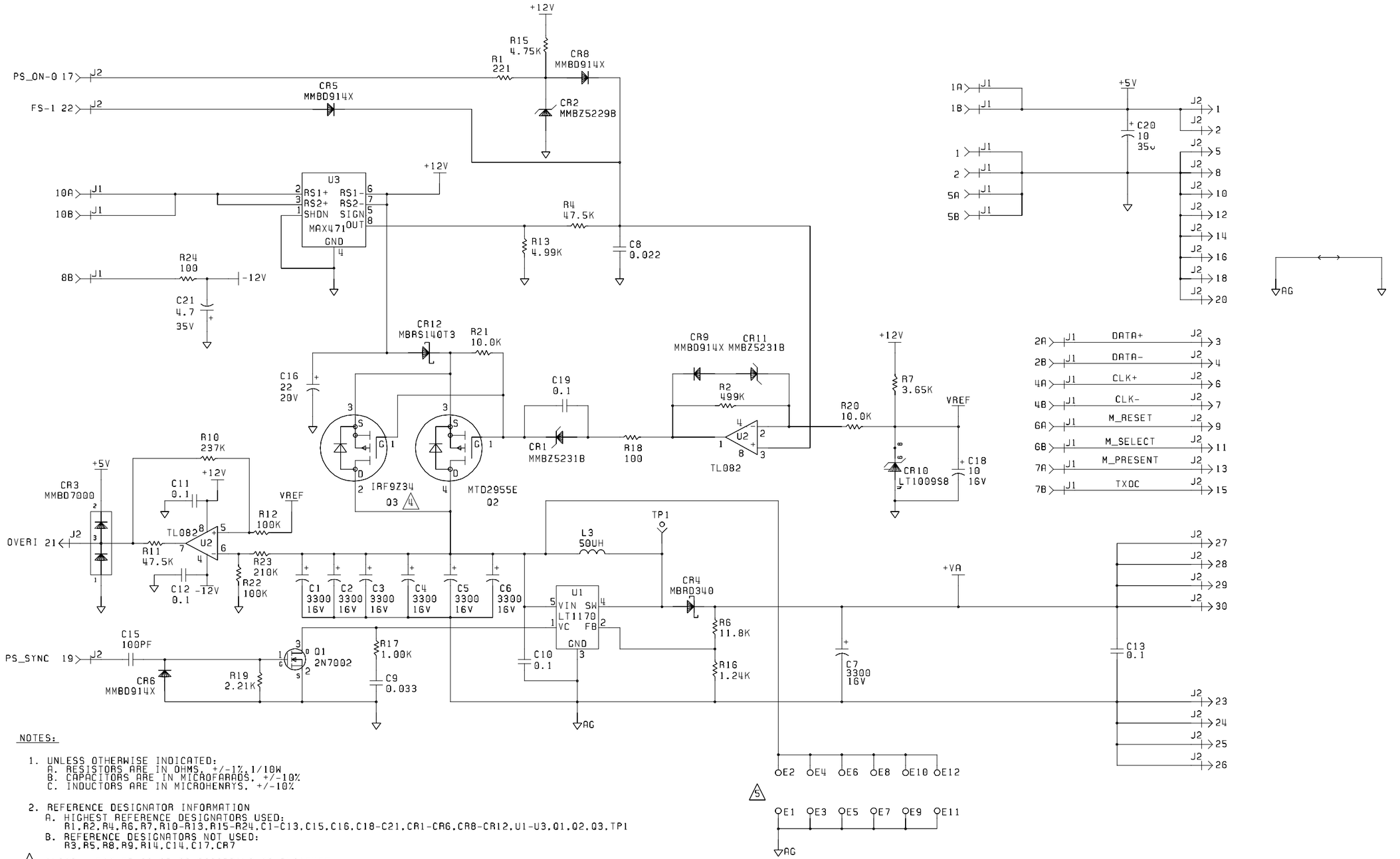
SC315-441 A
Recorder Digital PWA Schematic (5 of 7)



SC315-441 A
Recorder Digital PWA Schematic (6 of 7)



SC315-441 A
Recorder Digital PWA Schematic (7 of 7)



NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      R1,R2,R4,R6,R7,R10-R13,R15-R24,C1-C13,C15,C16,C18-C21,CR1-CR6,CR8-CR12,U1-U3,Q1,Q2,Q3,TP1
   B. REFERENCE DESIGNATORS NOT USED:
      R3,R5,R8,R9,R14,C14,C17,CR7

4 INSTALL EITHER Q2 OR Q3 ACCORDING TO PL315455.

5 ADDITIONAL PADS FOR ALTERNATE CAPACITOR BANK (C1-C6).

SC315-455 B
Recorder Power Supply PWA Schematic (1 of 1)